IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
MIDLAND/ODESSA DIVISION

REDSTONE LOGICS LLC, Plaintiff, v. MEDIATEK, INC. and MEDIATEK USA, INC. Defendants.	Case No. 7:24-cv-00029-DC-DTG

PLAINTIFF'S RESPONSIVE CLAIM CONSTRUCTION BRIEF

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I. Introduction

Defendant's indefiniteness arguments fall short of meeting the burden of clear and convincing evidence. While Defendant offers the declaration of Dr. Baker that the disputed terms are indefinite. Dr. Baker previously testified before the PTAB that he understood exactly what term covered. While parties may argue in the alternative, expert testify as to the *facts*. Dr. Baker's conflicting opinions render him unreliable and not credible. His opinions cannot satisfy Defendant's evidentiary burden.

Even if Dr. Baker's opinions are considered, Defendant's arguments remain fundamentally flawed. "Dynamically" and "periphery" are not terms of degree but are commonly understood in the art. While "substantially central" is a term of degree, the patent provides ample guidance for a POSITA to understand its scope.

II. Disputed Terms Requiring Construction

a. Term 1: "each processor core from the first/second set of processor cores is configured to dynamically receive a first/second supply voltage [from a power control block] and a first/second output clock signal"

'339 Patent Claims	Redstone's Proposed Construction	Defendant's Proposed Construction
Claims 1, 21	**Plain and ordinary meaning**	**Indefinite**[1]

Defendant argues because "configured to dynamically receive" does not have a common understanding in the field and "dynamically" is a "term of degree," the disputed term is indefinite. This argument is unfounded.

[1] Plaintiff notes that while Defendant MediaTek and Defendant NXP argue these three terms are indefinite and make similar arguments, the arguments are not identical and are supported by different experts.

First, the phrase "configured to dynamically receive" is plainly understandable to a POSITA. Both the advantages and difficulties of dynamically providing voltage and clock signals to processor cores in a multi-core processor were well known in the art by the time of the priority date. For example, the patent explains that "dynamically adjusting the power profile for a stripe in response to changes in computational requirements may reduce power consumption for a multi-core processor." '339 Patent at 3:16-20. Further, the face of the patent cites at least one paper detailing how to manage this dynamic change. *See* Dynamic Voltage and Frequency Scaling Circuits with Two Supply Voltages[2] ("Cheng[3]"). If a POSITA would understand dynamically *providing* voltage and clocks, they would also understand dynamically *receiving*, which is merely the complementary action.

While the exact phrase "configured to dynamically receive" is not found in the specification, that is not required. *See e.g. ESCO Grp. LLC v. Deere & Co.*, No. CV 20-1679-WCB, 2023 WL 4199413, at *14 (D. Del. June 22, 2023) (Bryson, C.J.). Defendant and Plaintiff agree that "configured to dynamically receive" is not some term of art with a specialized meaning separate and apart from its component terms. It merely refers to the set of processor cores being configured to receive changing voltage and clock signals, such as for jobs with differing computational demands.

Defendant's next argument that "dynamically" is a term of degree is no more availing. First, "dynamically" is never used as a threshold requirement, whether in the specification, the claims, or the art. Second, "dynamically" is a common term in the art to reference intentional

[2] This paper was cited on the face of the patent and therefore is intrinsic evidence. *V-Formation, Inc. v. Benetton Grp. SpA*, 401 F.3d 1307, 1311 (Fed. Cir. 2005).
[3] Cheng is included herewith as Ex. 1 to Mirzaie Declaration.

changes and is not used to reference mere fluctuations. *See e.g.* Ex. 2[4] at 41-42; 61-62; Cheng *generally*. Indeed, this is how the patent uses the term. *See* '339 Patent at 3:16-56. A POSITA would be readily familiar with the term.

Defendant's comparison to claim 5 is irrelevant. Claim 5's reference to "configured to receive one or more control signals" references a specific connection to "control blocks located in a periphery," not the overall configuration of a set of processor cores as in the independent claim. The cited language serves a different function than the disputed term. The language of claim 5 does not reference a changing signal as "dynamically" does. They are simply not comparable.

Defendant also has no reliable extrinsic evidence showing indefiniteness. Defendant relies on the declaration of Dr. Baker, who asserts that "a PHOSITA would not know whether 'dynamically' refers to changes … above a specific threshold or even what that threshold might be." Dkt. No. 29-1 at ¶40. But Dr. Baker himself confidently opined before the PTAB that two different references taught "*[d]ynamic* voltage and frequency scaling" and that "voltage … and the frequency of the processor may be *dynamically* modified" as a basis for combining references. Ex. 2 at 41-42 (emphasis added). When applying "configured to dynamically receive" to the prior art, Dr. Baker found no issue in determining that prior art purportedly teaching "'individually control/scale the voltage of each processor core []' so that the voltage supply may increase or decrease" thereby discloses the "dynamically receive" limitation. Ex. 2 at 61-62. This is incompatible with a POSITA not understanding what level of change is required for "dynamically" to be met. Dr. Baker recognized that "dynamically" is a readily understood term in the art, citing the term directly from the prior art. Ex. 2 at 41-42; 61-62. This sort of double-speak renders Dr. Baker's testimony entirely unreliable and not credible. *See e.g. Seigler v. Wal-Mart Stores Texas,*

[4] Declaration of R. Jacob Baker, PH.D., P.E. In Support of Petition for *Inter Partes* Review of U.S. Patent No 8,549,339.

L.L.C., 30 F.4th 472, 477 (5th Cir. 2022) (providing the "sham-affidavit doctrine" holds "affidavit testimony that is 'inherently inconsistent' with prior testimony" should be disregarded). Without his opinion evidence, Defendant has nothing and cannot meet its evidentiary burden.

Defendant has failed to show that "dynamically," a frequently used term in the art, is so vague that a person skilled in that art could not reasonably ascertain the meaning of "configured to dynamically receive." The patent sufficiently explains the context and purpose of the term. It is clear that it relates to the necessary configurations to receive changing power profiles.

b. Term 2: "located in a periphery of the multi-core processor"

'339 Patent Claims	**Redstone's Proposed Construction**	**Defendant's Proposed Construction**
Claims 5	**Plain and ordinary meaning**	**Indefinite**

Defendant next argues that "periphery" is also a term of degree. It is not. It is a relational term. In this case it defines an area in relation to the multi-core processor. By way of analogy, no one would suggest that "outdoors" is a term of degree because it is supposedly unclear whether a person in the process of walking through the door is "outdoors" or not. "Outdoors" is neither a term of degree nor vague, the hypothetical merely raises an edge case where the factual determination is difficult. The same is true of "periphery."

The Court's analysis need go no further. There is no vagueness introduced by any of the patent's figures. Figure 1 depicts a multi-core processor where the various cores are depicted as 102 with a potential set 150 of cores 152, 154, and 156. *See* '339 Patent at 2:4-40; 3:16-26. The specification provides "[i]n some implementations, the power control block 108 and the clock control block 110 may be arranged at two different sides of the multi-core processor 100 as shown in FIG. 1." '339 at 2:34-36. This shows where the edges of the multi-core processor are, with the

control blocks described at the edge of the multi-core processor. With the bounds of the multi-core processor so explained, a POSITA would readily ascertain where the periphery is.

Defendant's identification of Figure 3 as confusing the issue is simply unfounded. Figure 3 is a block diagram. '339 Patent at 1:31-33. Block diagrams do not depict the physical locations of components, they represent components as blocks and show connections and signal flows. Because a block diagram offers no insight into the physical arrangement of a component, its representational arrangement cannot conflict with the physical arrangements of other figures. A POSITA would simply not look to a block diagram for information on a periphery of the multi-core processor.

Once again, Dr. Baker tells one story to the PTAB and a different one to this Court. When identifying control blocks on the periphery of a multi-core processor, Dr. Baker had no issue in concluding that the periphery is "at a position above and away from the coherency manager," which he equated with the center of the processor. Ex. 2 at 85-86.

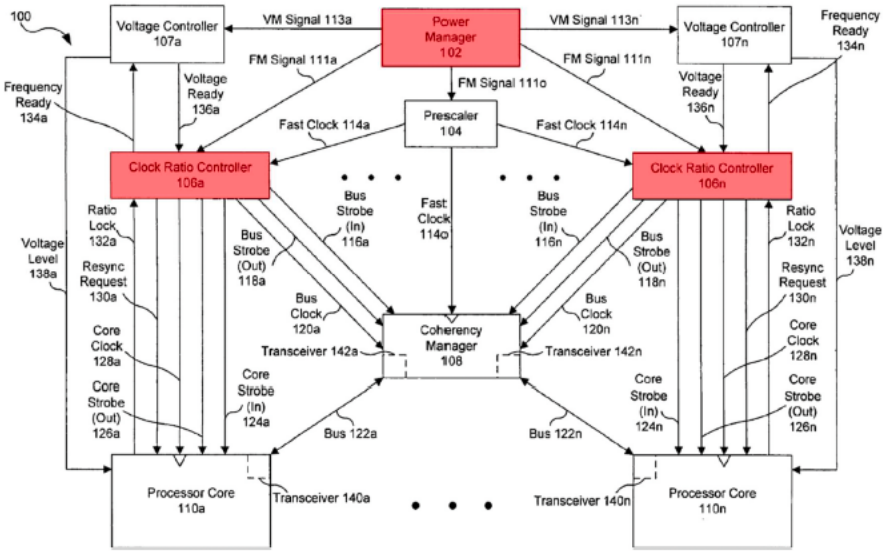

FIG. 1A of Knoth, annotated

Id. Although Dr. Baker again uses a block diagram that does not depict a physical architecture, he clearly demonstrated an understanding of "periphery." In fact, Dr. Baker based his understanding of "periphery" on the *exact* same sections of the '339 Patent that he now argues are unhelpful. *Compare* Dkt. No. 29-1 at 16-17 (citing '339 Patent at 2:20-40 as "not discuss[ing] where the periphery is located") *with* Ex. 2 at 87-88 (citing same as "teach[ing] the location of the one or more control blocks, [though not] how the positioning would affect their functionality"). This unreconcilable and conflicting testimony renders his declaration unreliable and not credible. *See Seigler*, 30 F.4th at 477. Because Defendant's indefiniteness argument hinges entirely on Dr. Baker's declaration, Defendant cannot meet its burden to establish indefiniteness.

A POSITA readily understand the scope of "located in a periphery of the multi-core processor." As noted above, "periphery" is a well-known relational term used in relation to a well-defined term "multi-core processor." The disputed term should be given its plain and ordinary meaning.

c. Term 3: "located in a common region that is substantially central to the first set of cores and second set of processor cores"

'339 Patent Claims	Redstone's Proposed Construction	Defendant's Proposed Construction
Claims 14	**Plain and ordinary meaning**	**Indefinite**

Here, Defendant's twofold argument that both "located in a common region" and "substantially central" are individually indefinite, both fail. Defendant contends "substantially central" is a term of degree without sufficient notice of scope while "common region" simply has no ascertainable meaning from the specification. Neither are true.

First, "located in a common region" is clear to a POSITA. Rather than merely relating to an undefined area, "region" is used throughout the patent to refer to sections of the multi-core processor. *See* '339 Patent at 2:20-21 ("The multi-core processor 100 may be further divided into regions.") The specification explains these regions may "correspond to rows of the two-dimensional array, and the regions may or may not be overlapping." *Id*. at 2:22-23. These "two-dimensional array[s]" are the rows of processors or stripes that can make up sets of processor cores. *Id*. at 2:24-27. This use is continued throughout the claims. *See e.g. id*. at Cl. 8 ("wherein the first set of processor cores are located in a first region of the multi-core processor, and the second set of processor cores are located in a second region of the multi-core processor.") A POSITA would understand that a "region" corresponds with the subdivision of the multi-core processor containing the claimed sets of processor cores.[5]

Understanding that the claimed "region" contains the control blocks and is a subdivision of the multi-core processor relating to sets of core processors, the meaning of "common region" becomes clear. "Common region," rather than being a term of art, merely references a region common to the first and second sets of processor cores. *See id*. at Cl. 14. While different architectures will dictate different forms for such a region, a POSITA would understand the scope of "common region."

Even Defendant recognizes "common region" refers to a part of the multi-core processor shared by the first and second sets of processor cores, though Defendant attempts to discredit it through claim differentiation. Dkt. No. 29 at 14-15. However, claim differentiation as a doctrine cannot be used to support a finding of indefiniteness. Claim differentiation creates a *rebuttable* presumption of non-redundant claims. *See Comark Communications, Inc. v. Harris Corp*., 156

[5] Again, Defendant cites Figure 3 as amplifying confusion. But as noted above, Figure 3 is a block diagram that a POSITA would not look to for guidance regarding the physical layout claimed.

F.3d 1182, 1187, 48 U.S.P.Q.2d 1001 (Fed. Cir. 1998) ("While we recognize that the doctrine of claim differentiation is not a hard and fast rule of construction, it does create a presumption that each claim in a patent has a different scope."). The Federal Circuit has explained that this cannon is not an absolute, "where neither the plain meaning nor the patent itself commands a difference in scope between two terms, they may be construed identically." *Power Mosfet Technologies, L.L.C. v. Siemens AG*, 378 F.3d 1396, 1409–10, 72 U.S.P.Q.2d 1129 (Fed. Cir. 2004). Here, if, as Defendant argues, claim 14 has an overlapping meaning with claim 9, that meaning is mandated by the plain meaning and the patent itself and thus the claims should be construed identically, not indefinitely. Even if claim differentiation could result in indefiniteness, claim differentiation is inapplicable. There are a variety of other differences between claim 14 and claim 9. For instance, claim 9 does not recite "one or more control blocks" or mandate where such a block is located. Claim 14 does. Further, claim 9 recites two regions, claim 14 recites only one. With so many differences between claim 9 and 14, there is no risk that the Court finding claim 14 definite would render any claim superfluous. Considering even Defendant recognizes the scope of "common region," "common region" cannot be the basis for finding claim 14 indefinite.

Defendant's alternative basis for indefiniteness fairs no better. For a "substantially" term to be definite, "[a]ll that is required is some standard for measuring the term of degree." *Exmark Mfg. Co. Inc. v. Briggs & Stratton Power Prods. Grp., LLC*, 879 F.3d 1332, 1346 (Fed. Cir. 2018). The patent provides that guidance.

First, the claim language itself provides guidance. The claimed control blocks are located in a "common region" that is substantially central to the first and second set of processor cores. A POSITA's understanding of what a "region" is, as explained above, guides where the contained

control blocks can be located. Because a "region" is a subdivision of the multi-core processor, a POSITA would understand that this is within the multi-core processor.

Second, the patent describes a number of embodiments with regard to the placement of control blocks. The patent describes three possibilities "two different sides of the multicore processor," "the same side of the multi-core processor," or "in a common area located near the center of the multi-core processor." '339 Patent at 2:31-40. Put differently, the patent describes putting the control blocks on the sides of the processor or within the processor. A POSITA would understand by contrast and example "substantially central" refers to not along the outside of the multi-core processor but the inside. When combined with a POSITA's understanding of "common region," a POSITA has a standard by which to measure "substantially central."

While Defendant attempts to muddy the water with reference to a distributed multi-core processor on a die, these arguments are faulty. Most notably, Defendant's proposal does not consider or recognize the role of the "common region." While the claimed invention can be distributed similarly to how Defendant describes, this example fails to consider the interconnections between the stripes such as the claimed "interface block" or the described interface circuit, *see* '339 at 2:9-19. Without these interconnections there is no common region for the control blocks to be located in. By ignoring these interconnections, a POSITA cannot ascertain the architecture of the multi-core processor to determine if the control blocks are substantially central or even outside. However, such an abstraction is non-functional. In a functional system, a POSITA would be able to ascertain the existence of a common region and the location of the control blocks in relation to it and the claimed multi-core processor.

Many of these points were made by Dr. Baker himself in his IPR declaration. For instance, Dr. Baker observed that "a 'region' is simply a spatial grouping of cores based on their physical

location in the multi-core processor." Ex. 2 at 104. However, he never applies that understanding here. As for what "substantially central" means, Dr. Baker again relied on the same language of the '339 Patent as with "periphery." *See* Ex. 2 at 87-88, 104-105. Notably, Dr. Baker had no difficulty ascertaining the scope of "substantially central" when it supported an invalidity argument, yet now that ascertaining that scope undermines his position, his stance has conveniently shifted. Dr. Baker's testimony regarding this term is unreliable and not credible. As the only evidence cited by Defendant, his testimony cannot meet its burden.

For these reasons, Defendant has not shown by clear and convincing evidence that Claim 14 is indefinite. Claim 14 should be given its plain and ordinary meaning.

III. Conclusion

For the reasons provided above, all disputed terms should be given their plain and ordinary meaning. Defendant has failed to meet its burden to show any term is indefinite.

Dated: January 8, 2025

Respectfully submitted,

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CERTIFICATE OF SERVICE

I certify that on January 8, 2025, a true and correct copy of the foregoing document was electronically filed with the Court and served on all parties of record via the Court's CM/ECF system.

/s/ Reza Mirzaie
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